IN THE SPECIFICATION

Please amend paragraph 61 as shown.

[0061] The taps **305**, ~~**306**~~ **307** of the shift registers **304**, **306** in a Gold code generator **300**, in essence, determine the sequence of chips generated by the Gold code generator **300**. As is well known to those in the art, the sequence of chips is a repeating pattern that repeats after a number of generated chips. The initial value that loaded into the Gold code generator **300** by load logic **202** determines, in essence, what part of that repeating sequence will be generated by the Gold code generator **300**. By varying the initial values loaded in the plurality of Gold code generators of Figures 2 and 3, each generator may be configured to generate one of the set of possible Gold codes for the shift register tap configuration. One of the plurality of generators will therefore correlate with the sequence being generated by the corresponding transmitter thus allowing rapid code acquisition.

Please amend paragraphs 65 and 66 as shown to correct instances of ":=" to appear as "=".

[0065] In one aspect hereof, the *j*-th stage of each *N*-stage Gold code generator may be loaded as a function of the *j*-th received chip where *j* ranges from 0 through *N*-1 as follows:

$$\text{if } (C_j == 0) \text{ then } A_{i,N-1-j}[[:]] = 0;\ B_{i,N-1-j}[[:]] = 0 \quad \text{OR} \quad A_{i,N-1-j}[[:]] = 1;\ B_{i,N-1-j}[[:]] = 1$$

$$\text{else } A_{i,N-1-j}[[:]] = 0;\ B_{i,N-1-j}[[:]] = 1 \quad \text{OR} \quad A_{i,N-1-j}[[:]] = 1;\ B_{i,N-1-j}[[:]] = 0$$

where i ranges from 0 through 2^N-1 as determined by indexing logic. As noted above, such indexing logic may use any of numerous well known indexing techniques including, for example, simple modulo arithmetic to assure that all 2^N generators are pre-loaded with a different value of the 2^N possible pre-load values. The indexing logic may select from the two optional pre-load values in response to each received chip and according to the indexing technique to assure all possible values are pre-loaded in the generators. Such indexing techniques and associated circuits would be readily recognized by those skilled in the art.

[0065] In another aspect hereof, the A and B registers of the 2^N Gold code generators each having *N* stages may be loaded as follows in response to the indicated received chip values C_j:

$$A_{i,N-1-j}[[:]] = \frac{1-(-1)^{floor(i\cdot 2^{-j})}}{2} \qquad (1)$$

$C_j[[:]] = 0$	$B_{i,N-1-j}[[:]] = A_{i,N-1-j}$
$C_j[[:]] = 1$	$B_{i,N-1-j}[[:]] = \mathrm{mod}(A_{i,N-1-j}+1,2)$

(2)

where: *i* is a range variable from 0 to 2^N-1, C_j is the *j*-th received chip, *j* = 0 to *N*-1, and floor(x) is the integer value of x. It may be noted that in the above pre-loading aspect, the values in the 1-register are a function of the chip index "*j*" but not the chip value "C_j." Those skilled in the art will note that, in accord with equation 1 above, the value loaded in the a-register of each Gold code generator is therefore not dependent on the received chip value. Therefore, the a-register of each generator may be pre-loaded at initialization of the receiver and need not be modified in response to received chips. The values to be pre-loaded into each a-register may therefore be statically saved in a memory component such as a read-only memory (ROM) or other similar memory component.